Organic ElectroLuminescent Device

Compensated Pixel Driver Circuit

The present invention relates to an organic electroluminescent device and particularly to a compensated pixel driver circuit thereof.

An organic electro-luminescent device (OELD) consists of a light emitting polymer (LEP) layer sandwiched between an anode layer and a cathode layer. Electrically, this device operates like a diode. Optically, it emits light when forward biased and the intensity of the emission increases with the forward bias current. It is possible to construct a display panel with a matrix of OELDs fabricated on a transparent substrate and with one of the electrode layers being transparent. One can also integrate the driving circuit on the same panel by using low temperature polysilicon thin film transistor (TFT) technology.

In a basic analog driving scheme for an active matrix OELD display, a minimum of two transistors are required per pixel (Figure 1): T_1 is for addressing the pixel and T_2 is for converting the data voltage signal into current which drives the OELD at a designated brightness. The data signal is stored by the storage capacitor $C_{storage}$ when the pixel is not addressed. Although p-channel TFTs are shown in the figures, the same principle can also be applied for a circuit with n-channel TFTs.

There are problems associated with TFT analog circuits and OELDs do not act like perfect diodes. The LEP material does, however, have relatively uniform characteristics. Due to the nature of the TFT fabrication technique, spatial variation of the TFT characteristics exists over the entire panel. One of the most important considerations in a TFT analog circuit is the variation of threshold voltage, ΔV_T, from device to device. The effect of such variation in an OELD display, exacerbated by the non perfect diode behaviour, is the non-uniform pixel

brightness over the display panel, which seriously affects the image quality. Therefore, a built-in compensation circuit is required.

A simple threshold voltage variation compensation, current driven, circuit has been proposed. The current driven circuit, also known as the current programmed threshold voltage compensation circuit is illustrated in figure 2A. In this circuit, T_1 is for addressing the pixel. T_2 operates as an analog current control to provide the driving current. T_3 connects between the drain and gate of T_2 and toggles T_2 to be either a diode or in saturation. T_4 acts as a switch. Either T_1 or T_4 can be ON at any one time. Initially, T_1 and T_3 are OFF, and T_4 is ON. When T_4 is OFF, T_1 and T_3 are ON, and a current of known value is allowed to flow into the OELD, through T_2. This is the programming stage because the threshold voltage of T_2 is measured with T_2 operating as a diode (with T_3 turned ON) while the programming current is allowed to flow through T_1, through T_2 and into the OELD. T_3 shorts the drain and gate of T_2 and turns T_2 in to a diode. The detected threshold voltage of T_2 is stored by the capacitor C_1 connected between the gate and source terminals of T_2 when T_3 and T_1 are switched OFF. Then T_4 is turned ON, the current is now provided by V_{DD}. If the slope of the output characteristics were flat, the reproduced current would be the same as the programmed current for any threshold voltage of T_2 detected. By turning ON T_4, the drain-source voltage of T_2 is pulled up, so a flat output characteristic will keep the reproduced current the same as the programmed current. Note that ΔV_{T2} shown in figure 2A is imaginary, not real.

A constant current is provided, in theory, during the active programming stage, which is t_3 to t_4 in the timing diagram shown in figure 2A. The reproduction stage starts at t_6 and ends at t_1 of the next cycle.

In practice, there is always a slope in the output characteristics, so the reproduced current is not the same as the programmed current. This issue limits the device channel length of the polysilicon TFTs because of the increase of the short channel effect in polysilicon TFTs when the device channel length gets smaller. Simulations show that the variation between the reproduced current and programmed current is unacceptable for L = 4μm and below. This limitation on the design of transistor T_2 is a very serious practical problem, especially when small data currents are used. It is therefore important to find a technique that will provide good compensation in short channel devices.

The driving waveforms used are shown in timing chart fashion in figure 2B. The threshold voltage V_T shown at the bottom of figure 2B is that for transistor T_2. As can be seen from figure 2B, this threshold voltage has a range of −1V to +1V. Such a range is much larger than the variation ΔV_T across a practical OELD matrix.

Typical variation between the reproduced current and programmed current supplied to the OELD is illustrated in figure 2C. Figure 2C illustrates three cycles of OELD current supply: one from 0 to 30μs, one from 30μs to 60μs, and one from 60μs to 90μs. The first half of each of these cycles is the programming stage and the second half of the cycle is the reproduction stage. It is to be noted that the current output levels in the reproduction stage compared with those in the corresponding program stage are remarkably different from each other.

According to a first aspect of the present invention there is provided a compensated pixel driver circuit for an organic electroluminescent device, wherein the circuit comprises a unity gain buffer. Preferably the unity gain buffer is implemented as an operational amplifier.

According to a second aspect of the present invention there is provided a method of compensating the current supply to an organic electroluminescent pixel comprising the step of using a unity gain buffer to provide a self adjusting load.

According to a third aspect of the present invention there is provided an organic electroluminescent display device comprising one or more compensated pixel driver circuits according to the first aspect of the invention.

Embodiments of the present invention will now be described by way of example only and with reference to the accompanying drawings, in which:-

Figure 1 shows a conventional OELD pixel driver circuit using two transistors,

Figure 2 shows a current programmed OELD driver with threshold voltage compensation,

Figure 3 shows a compensated pixel driver circuit according to an embodiment of the present invention,

Figure 4 is a table of requirements for one specific example of an operational amplifier which can be used in the circuit of figure 3,

Figure 5 is an example of a circuit for implementing the operational amplifier shown in figure 3,

Figure 6 is a graph illustrating the unity-gain buffer characteristics of the compensating circuit of figure3,

Figure 7 is a graph illustrating the total required supply current,

Figure 8 is a driving waveform timing diagram, and

Figure 9 illustrates the current output to the OELD using the circuit of figure 3.

A compensated pixel driver circuit according to an embodiment of the present invention is shown in figure 3. Compared with the circuit of figure 2, there is added an operational amplifier OpAmp A, a capacitor C_2 and a transistor T_5. As shown in figure 3, V_{out} of the OpAmp is connected to the inverting input V_- thereof. The OpAmp thus has unity gain. Capacitor C_2 ensures a sample and hold function and transistor T_5 acts as a control switch to store the voltage on C_2. In effect the circuit provides a self-adjusted load or voltage source (V_{DD}) and by thus

holding the operative voltage constant the effect of the slope in the output characteristics can be avoided. In it's generic form, the OpAmp A is a unity gain buffer having it's input connected to the source–drain path of transistor T_5 and it's output connected to the source–drain path of transistor T_4, the input being connected to ground via capacitor C_2.

As shown in figure 3, a TFT operational amplifier configured as a sample and hold circuit is used to provide a variable V_{DD} so that the drain-source voltage of T_2 in the reproduction stage is the same as that during the programming stage. During the programming stage, the voltage at the source of T_2 is passed to the storage capacitor C_2 at the input of the unity-gain OpAmp. The output of the OpAmp faithfully reproduces the voltage and also provides the current to the OELD through T_2. The driving waveform is the same as that for the circuit of figure 2.

The program current path is from V_{DD2} through node V_4, T_1, T_2 and the OELD. The reproduction current path is from V_{DD1}, through the OpAmp, V_{out}, T_4, node V_4, T_2 and the OELD.

In the circuit of figure 3, the voltage at point V_4 is substantially the same in the reproduction cycle to the voltage at that point in the programming cycle. Additionally, a very high Open-Loop Gain (OLG) is not required in contrast to usual TFT circuits. An advantage of the embodiment of the present invention shown in figure 3 is that the current flow to the OELD during the reproduction cycle is less sensitive to the variation in the output V_{out} of the OpAmp than ΔV_{T2} detection of the same percentage error. Furthermore, the OpAmp design constraints are not stringent.

Figure 5 is a circuit diagram of one arrangement for implementing the OpAmp shown in figure 3. The specific requirements for this circuit are shown in the table of figure 4. Of particular note is the minimal off-set voltage. Typically this might be a few millivolts, in contrast

to the variation of several volts which may typically arise in the conventional arrangement due to the slope of the output characteristics. The circuit of figure 5 essentially consists of a differential pair circuit and a driver. The differential pair circuit comprises the top two transistors connected to the V_{DD1} rail, the respective transistors having their gates providing the two input terminals of the OpAmp, and the transistor whose gate receives V_{bias1}. The output driver comprises a transistor receiving V_{bias2} at its gate and a transistor connected between the V_{DD1} rail and V_{out}.

All of the transistors of the circuit of figure 5 are TFTs having a channel length of 10μm (in contrast to T_2). This channel length avoids the devices being stressed by the high value of V_{DD}. The transistor connected between the V_{DD1} rail and V_{out} has a channel width of 100μm in order to ensure sufficient current output. The area required to implement the circuit of figure 5 can be reduced by varying the W/L absolute size ratio of the transistors, subject to a corresponding reduction in the maximum drive current. The space occupation value of 270μm x 70μm given in the table of figure 4 can, for example, be reduced to approximately 130μm x 10μm, subject to a reduction in the maximum drive current from 5μA to 1.5μA. However, in practice a maximum drive current of 1μA might suffice (as indicated in figure 4).

In the specific example given, the current I_{DP} flowing through the differential pair circuit has a maximum value of 1μA and the current I_{OB} flowing through the driver circuit has a maximum value of 5μA. The additional current required by the presence of the OpAmp is thus minimal.

Figure 6 is a graph illustrating the unity-gain buffer characteristics of the compensating circuit of figure 3. As shown, the plot of V_{out} against V_+ is the same for both the load and the

no-load conditions. The load condition is 5MΩ, which corresponds to a current of 1μA through the OELD.

The total current supply required by the OpAmp of figure 3, in one specific example, is shown in figure 7. The total current supply required is that required by the differential pair circuit (figure 5), that required by the OpAmp driver circuit (figure 5) and that required to drive the OELD. Again load (5MΩ) and no-load conditions are shown.

The driving waveforms used with one implementation of the circuit of figure 3 are shown in timing chart fashion in figure 8. Of course, the threshold voltage V_T shown at the bottom of figure 8 is that for transistor T_2. As can be seen from figure 8, this threshold voltage has a range of −1V to +1V. Such a range is much larger than the variation ΔV_T across a practical OELD matrix. Threshold variation ΔV_T in other transistors (T_1, T_3, T_4, T_5) have little effect as they are used as switches and operate under voltage ranges greater than ΔV_T.

The output current supplied to the OELD using the circuit of figure 3 is illustrated in figure 9. Figure 9 illustrates three cycles of OELD current supply: one from 0 to 30μs, one from 30μs to 60μs, and one from 60μs to 90μs. The first half of each of these cycles is, of course, the programming stage and the second half of the cycle is the reproduction stage. In each cycle, five different program currents are illustrated (ie vertically – at 0.2, 0.4, 0.6, 0.8 and 1.0). It is to be noted that the current output levels in the reproduction stage compared with those in the corresponding program stage are remarkably close. The comparison is slightly less good for larger program currents, but is still relatively small. Moreover, the difference can be predicted (as shown in figure 9) and can therefore be included in a gamma compensation (eg use 1.1μA instead of 1μA in the programming stage).

It will be apparent to persons skilled in the art that variations and modifications can be made to the arrangements described with respect to figure 3 to 9 without departing from the scope of the invention.